REMARKS

In the Office Action dated March 21, 2007, claims 1-25 were presented for examination. The Examiner rejected claims 1-11 under 35 U.S.C. §101. The Examiner rejected claims 1-25 under 35 U.S.C. §102(b).

The following remarks are provided in support of the pending claims and responsive to the Office Action of March 21, 2007 for the pending application.

I. Rejection Under 35 U.S.C. §101

In the Office Action dated March 21, 2007, the Examiner rejected claims 1-11 under 35 U.S.C. §101 indicating the claims are directed to non-statutory subject matter. More specifically, the Examiner has indicated that the language of claim 1, and claims 2-11, as being directed to an abstract idea. Applicant has amended claim 1 in compliance with the suggested language provided by the Examiner.[1] Accordingly, Applicant respectfully requests that the Examiner remove the rejection of claims 1-25 under 35 U.S.C. §101

II. Rejection under 35 U.S.C. §102(b)

Claims 1-25 were rejected under 35 U.S.C. §102(b) as being anticipated by *Robertson*, U.S. Patent No. 5,850,632.

Applicant hereby incorporates the comments and remarks made to the *Robertson* patent '632 in response to the prior Office Actions and the Appeal Brief.

The Examiner has asserted that program counter register of *Robertson* is equivalent to the pointer claimed by Applicant. Furthermore, the Examiner has asserts that the claims do not prohibit the shared resource from including the program counter register. Besides the double negatives placed in the confusing language of the Examiner, a program counter is local to a CPU. A program counter is "a register in the control unit of the CPU that is used to keep track of the address of the current or next instruction."[2] As clearly shown, a program counter is a hardware element that is directly associated with an instruction and is local to the CPU.

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[1]See Office Action, page 3.

[2]See Exhibit E.

Applicant's amended claims, as supported by the specification, clearly teach a pointer stored in a shared resource with the shared resource being stored in shared memory. Based upon the definition of a program counter, it is not stored in shared memory. Rather, the program counter is local to the control unit of the CPU. Clearly, *Robertson* does not expressly or inherently teach use of a pointer in the manner claimed by Applicant, *i.e.* stored in shared memory. The pointer is not a program counter, and a program counter of *Robertson* is not the pointer of Applicant. These are not interchangeable items, as they are used for different purposes to support different functions. Accordingly, it is Applicant's position that the Examiner is giving an interpretation to the terms of the claim beyond the metes and bounds of the claims, and hereby respectfully requests removal of the rejection of claims 1-25 under 35 U.S.C. §102(b).

V. Conclusion

Applicant believes that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. The amendment to the claims submitted herein does not require an additional search, since the limitations merely clarify those elements previously claimed. Accordingly, Application respectfully requests entry of the amendment to the claims, that the Examiner indicate allowability of claims 1-25, and that the application pass to issue. If the Examiner believes, for any reason, that personal communication will expedite prosecution of the application, the Examiner is hereby invited to telephone the undersigned at the number provided.

For the reasons outlined above, withdrawal of the rejection of record and an allowance of this application are respectfully requested.

Respectfully submitted,
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program counter

A register in the control unit of the CPU that is used to keep track of the address of the current or next instruction. Typically, the program counter is advanced to the next instruction, and then the current instruction is executed. Also known as a "sequence control register" and the "instruction pointer." See address register and instruction register.

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